

SYSTEM AND METHOD FOR DATA RETENTION WITH REDUCED  
LEAKAGE CURRENT

Abstract of the Disclosure

In embodiments, a data-retention circuitry comprises data-retention inverters in a feedback loop, an isolation subcircuit to isolate the inverters from a pass-gate subcircuit in response to a sleep signal, and a supply-switching subcircuit to provide current to the data-retention inverters from a supplemental voltage supply through a well tap during a standby mode. The supply-switching subcircuit switches from a regular voltage supply to the supplemental voltage supply in response to the sleep signal.

"Express Mail" mailing label number: EV332569975US  
Date of Deposit: June 27, 2003

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